A Practical Switching Loss Model for Buck Voltage Regulators

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***Abstract*—In this paper, a review of switching loss mechanisms for synchronous buck voltage regulators (VRs) is presented. Following the review, a new simple and accurate analytical switching loss model is proposed for synchronous buck VRs. The model includes the impact of common source inductance and switch parasitic inductances on switching loss. The proposed model uses simple equations to calculate the rise and fall times and piecewise linear approximations of the high-side MOSFET voltage and current waveforms to allow quick and accurate calculation of switching loss in a synchronous buck VR. A simulation program with integrated circuit emphasis (Spice) simulations are used to demonstrate the accuracy of the voltage source driver model operating in a 1-MHz synchronous buck VR at 12-V input, 1.3-V output. Switching loss was estimated with the proposed model and compared to Spice measurements. Experimental results are presented to demonstrate the accuracy of the proposed model.**

***Index Terms*—DC–DC power conversion, modeling, MOSFETs.**

I. Introduction

IN ORDER to optimally design a high-frequency switching converter, engineers and researchers begin their design by estimating the losses in a design file that is typically created using a spreadsheet, or other mathematical softwares. Device datasheet values and analytical models are used to calculate the losses. Using the loss models, many design parameters and components are compared to achieve a design with the optimal combination of efficiency and cost.

Analytical switching loss models use closed-form mathematical equations. Most often, piecewise linear turn-on and turn-off waveforms are used, or simplified equivalent circuits are used to derive switching loss equations. These methods yield closed-form mathematical expressions that can be used easily to produce optimization curves within a design file. The challenge with analytical modeling is to improve accuracy while minimizing complexity.

One of the most popular analytical switching loss models is the piecewise linear model presented in [1]. This model is referred to as the conventional model and is later used as a benchmark for comparison purposes with the proposed model. This model enables simple and rapid estimation of switching loss; however, the main drawback is that it neglects the switching loss dependences due to parasitic inductances. Typically, this model predicts that turn-on and turn-off loss are nearly similar in magnitude. However, in a real converter operating at a high switching frequency, the model is highly inaccurate since turn-off loss is much larger due to parasitic inductances.

A comprehensive analytical switching loss model for voltage source drive is presented in [2] and a model for current source drive is presented in [3]. These models are an extension of the model presented in [4], with the advantage that they provide accurate characterization of switching loss when common source inductance is included. Common source inductance is inductance in the source lead of a power MOSFET that is common to the power train circuit and driver. The main drawback of the models in [2]–[4] is their complexity.

The synchronous buck remains the topology of choice for voltage regulators (VRs) in today's computers [5]–[19]. However, in order to properly model switching loss in a buck VR, a detailed understanding of the impact of MOSFET gate capacitance, common source inductance, other parasitic inductance, and load current on switching loss is necessary. This is most easily accomplished through careful examination of waveforms through simulation and experiments, which are included in Section II, following the approach presented in [5].

In Section III, a new switching loss model is proposed with the goal of maintaining the relative simplicity of the very popular conventional model in [1], while improving the accuracy for high-frequency synchronous buck with parasitic circuit inductances, including common source inductance. In particular, the model predicts the large decrease in turn-on loss and increase in turn-off loss that occurs as undesired circuit parasitic inductance increases. The proposed model is compared to the conventional model and simulation program with integrated circuit emphasis (Spice) simulation results in Section IV. The model validation with experimental results are presented in Section V. The proposed model is then extended to current source drivers [11]–[13] in Section VI. The conclusions are presented in Section VII.

II. Impact of Parasitic Inductance and Load Current

A synchronous buck converter is illustrated in Fig. 1. In a synchronous buck VR, it is well known that the input voltage, load current, and high-side (HS) MOSFET gate-to-drain charge influence switching loss in the HS MOSFET. In addition, the inductances associated with the device packaging and printed circuit board (PCB) traces also contribute significantly to HS

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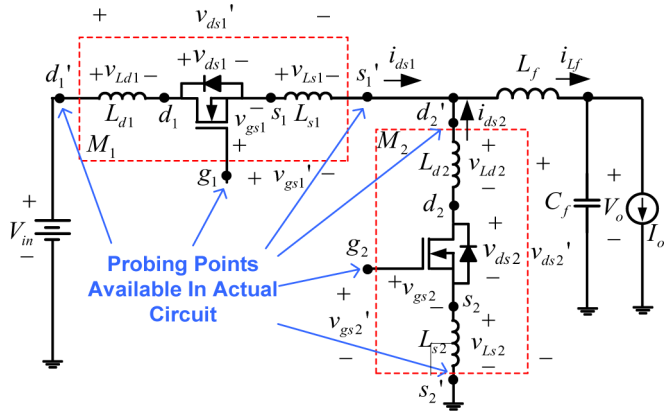


Fig. 1. Synchronous buck VR with parasitic inductances.

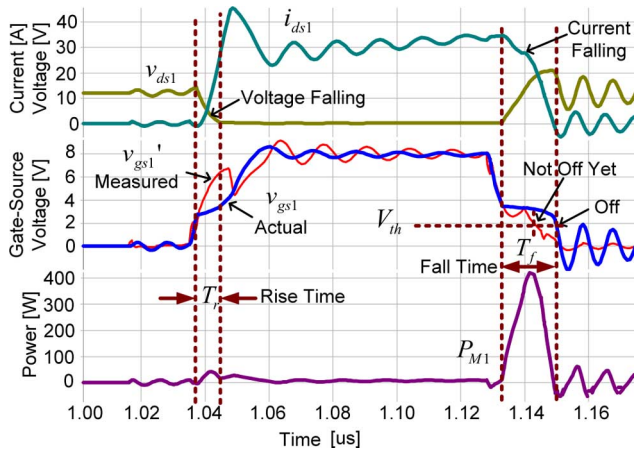


Fig. 2. Synchronous buck VR HS MOSFET waveforms (top) actual drain–source voltage v_{ds1} and drain current i_{ds1}; (middle) measured gate–source voltage v'_{gs1} and actual gate–source voltage (bold) v_{gs1}; (bottom) HS MOSFET power $v_{ds1}i_{ds1}$.

MOSFET switching loss. It is noted that the synchronous rectifier (SR) switches with near zero switching loss.

The synchronous buck in Fig. 1 includes parasitic drain and source inductances for the HS MOSFET M_1 and SR MOSFET M_2. It can be assumed that the source inductances L_{s1} and L_{s2} are common to their respective drive signals. Any other inductance in the source that is not common to the source is assumed to be lumped with the drain inductances L_{d1} and L_{d2}. These inductances have a significant impact on the switching loss behavior in high-frequency synchronous buck VRs.

During the switching transitions, the HS MOSFET operates in the saturation (linear) mode as a dependent current source, simultaneously supporting the current through the device and voltage across it. At turn-on and turn-off, the gate-source voltage v_{gs1} is held at the plateau voltage $V_{\rm pl}$ by the feedback mechanism provided by the voltage across the common source inductance v_{Ls1}, i.e., neglecting the internal MOSFET gate resistance $v'_{gs1} = V_{cc} = v_{gs1} + v_{Ls1} = V_{\rm pl} + v_{Ls1}$.

Simulation waveforms for a buck VR at 12 V input, 30 A load, 8 V drive voltage, and 1 MHz switching frequency are illustrated in Fig. 2. The top curves are the HS MOSFET switch current i_{ds1} and actual drain-to-source voltage v_{ds1}. The second set of curves are the v_{gs1} (actual) and v'_{gs1} (measured; $v'_{gs1} = v_{gs1} + v_{Ls1}$) waveforms, which are included to demonstrate that measuring v'_{gs1} in the laboratory provides an inaccurate representation of the switching times. The bottom curve is the power loss in the MOSFET $P_{M1} - v_{ds1}i_{ds1}$. Typically, parasitic inductance values for common package types are provided by the semiconductor manufacturers in application notes [6] and [7], and range from approximately 250 pH to 1 nH, depending on the package type. Matched inductances of 500 pH each for the four inductances were used in the simulation.

As can be observed from the circuit in Fig. 1 and the waveforms in Fig. 2, at turn-on, as the HS MOSFET current increases, v_{Ls1} is positive in the direction noted, so this voltage subtracts from the V_{cc} voltage applied to the gate, enabling $v_{gs1} = V_{\rm pl}$ while the MOSFET operates in the saturation mode. At the same time, the four parasitic inductances provide a current snubbing effect, which virtually eliminates turn-on switching loss enabling a near zero current switching (ZCS) turn-on. During this transition, the rise time T_r is dictated by the gate driver's ability to charge the MOSFET gate capacitances (C_{iss} from $V_{\rm th}$ to $V_{\rm pl}$ and C_{gd} to $V_{\rm in}$), which is defined in this paper as the time for v_{ds1} to fall to zero. Then, it is assumed that this time is independent of the time it takes i_{ds1} to rise to its final value equal to the buck inductor current, i.e., after T_r, i_{ds1} be less than the buck inductor current.

At turn-off, as the HS MOSFET current decreases, v_{Ls1} is negative in the direction noted in Fig. 1, so this voltage subtracts from the low-impedance source voltage (ideally zero volts) applied to the gate, enabling $v_{gs1} = V_{\rm pl}$ while in the saturation mode. During this transition, the fall time T_f is defined as the time for the HS MOSFET current to fall from the buck inductor current to zero. This time is dictated by both the gate driver's ability to discharge the MOSFET gate capacitances (C_{gd} from $V_{\rm in}$, and C_{iss} from $V_{\rm pl}$ to $V_{\rm th}$) and the four parasitic inductances, which prolong the time for i_{ds1} to fall to zero by limiting di_{ds}/dt.

As alluded to in the previous two paragraphs, the MOSFET and trace parasitic inductances have vastly different effects at turn-on and turn-off. At turn-on, the inductances provide a current snubbing effect, which decreases turn-on switching loss. At turn-off, the inductances increase the turn-off loss by prolonging T_f. In addition, as load current increases, T_f increases, so turn-off losses increase proportionally to I_0^2[proportional to I_o and $T_f(I_o)$]. In contrast, at turn-on, the load current magnitude has ideally no effect on the T_r. Therefore, in real circuits, turn-off loss is much greater than turn-on loss, which is clearly evident in the P_{M1} power loss waveform in Fig. 2.

Another important point to note from Figs. 1 and 2 is that in a real circuit, the board-mounted packaged inductances are distributed within the MOSFET devices. Therefore, when probing in the laboratory, one only has access to the external terminals g_1, s'_1, and d'_1' for the HS MOSFET and g_2, s'_2, and d'_2 for the SR. However, the actual nodes that provide waveform information relevant to the switching loss are at the unavailable internal nodes s_1 and d_1 for the HS MOSFET. Using the plateau

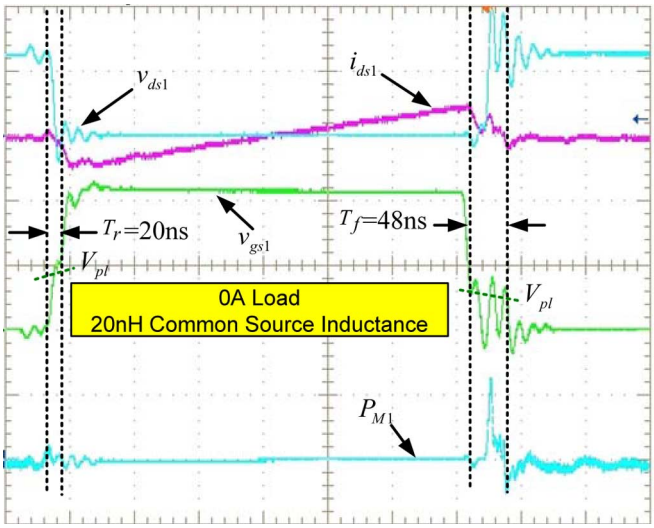


Fig. 3. Switching waveforms at 0 A load and 20-nH common source inductance (80 ns/division; v_{ds1}: 10 V/division; i_{ds1}: 5 A/division; v_{gs1}: 5 V/division; P_{M1}: 50 W/division).

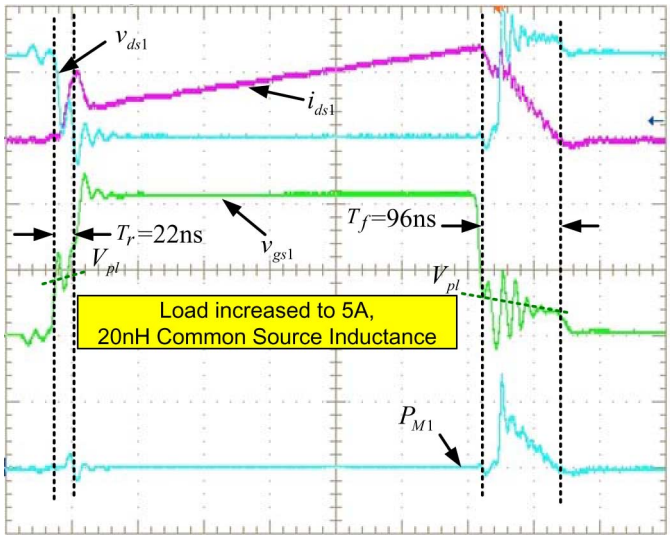


Fig. 4. Switching waveforms at 5 A load and 20-nH common source inductance (80 ns/division; v_{ds1}: 10 V/division; i_{ds1}: 5 A/division; v_{gs1}: 5 V/division; P_{M1}: 200 W/division).

portion of the measured gate–source voltage v'_{gs1} to determine the switching loss times is misleading since the induced voltage across L_{s1} is included. Probing v'_{gs1} in the laboratory, one would observe a negligible T_r at turn-on and a turn-off T_f less than one-half of the actual T_f. The actual v_{gs1} waveform, which cannot be measured in a real circuit, more clearly illustrates the plateau portions in the rise and fall times.

To demonstrate the effects of load current and common source inductance, experimental testing was done at a reduced frequency of 200 kHz, with the source connection cut and a wire inserted in the common source path to measure the MOSFET current. Measurement waveforms are illustrated in Figs. 3 and 4, where the load current has been increased from 0 to 5 A. With this method, the inductance of the wire (approximately 20 nH) is much greater than the approximate total package inductance of

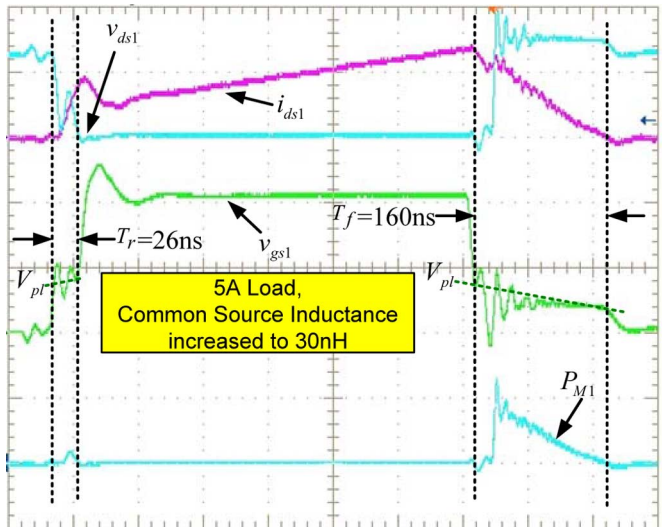


Fig. 5. Switching waveforms at 5 A load with 30-nH common source inductance (80 ns/division; v_{ds1}: 10 V/division; i_{ds1}: 5 A/division; v_{gs1}: 5 V/division; P_{M1}: 200 W/division).

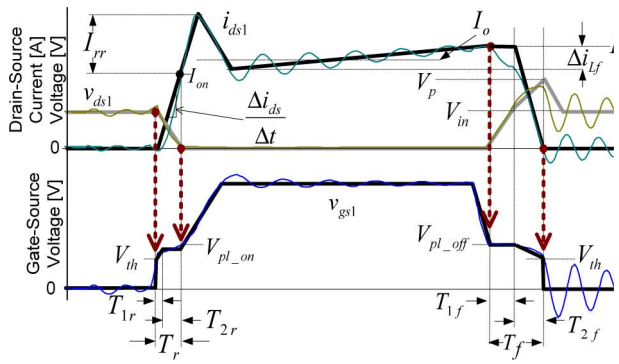


Fig. 6. Synchronous buck HS MOSFET waveforms with piecewise linear approximations of these waveforms in bold.

1 nH, so the package inductance can be neglected, allowing for measurement of v_{gs1} and v_{ds1}. As stated previously, it is noted that as load current increases from 0 to 5 A, T_r remains nearly unchanged from 20 to 22 ns, but T_f increases significantly from 48 to 96 ns. In addition, at a constant load current of 5 A, as illustrated in Fig. 5, as L_{s1} increases to 30 nH (using a longer 3-in wire), T_r remains relatively unchanged from 22 to 26 ns, while T_f further increases from 96 to 160 ns. It is noted that in Figs. 3–5, the v_{ds1} rise at turn-off appears to be steep and nearly rectangular due to the time scale; however, its actual rise is triangular, as will be illustrated in Fig. 6.

From knowledge of the circuit operation and observation of the experimental results presented, three important observations and conclusions can be made.

1) In a practical synchronous buck VR, turn-off loss is much greater than turn-on loss since the circuit inductances provide a current snubbing effect, which decreases and virtually eliminates turn-on switching loss, but increases the turn-off loss by prolonging T_f. In addition, the inductor ripple current decreases the current at turn-on and increases the current at turn-off, which further reduces

turn-on switching loss and increases turn-off switching loss.

2) T_r is dictated by the time for the voltage to fall to zero and is independent of the final value of the current. In addition, load current has negligible impact on T_r, while common source inductance has only a small impact, since as L_{s1} increases, the current di_{ds}/dt decreases.
3) T_f is dictated by the time for the current to fall to zero. Load current, common source inductance, and other circuit parasitic inductances (i.e., $L_{d1}, L_{s2},$ and L_{d2}) increase T_f.

III. Proposed Switching Loss Model

Typical switching waveforms for a synchronous buck VR are illustrated in Fig. 6. The proposed model uses the piecewise linear approximations (noted with thicker bold lines) of the switching waveforms in Fig. 6. Turn-on switching loss occurs during T_r and turn-off switching loss occurs during T_f. The key to the model is prediction of the turn-on current $I_{\rm ON}$, the rise and fall times T_r and T_f, the reverse recovery current, I_{rr}, the magnitude of the rising current slope $\Delta i_{ds}/\Delta t$, and the current drop Δi_{1f} when v_{ds1} rises to $V_{\rm in}$ at turn-off. The goal of the proposed model is to calculate the switching loss with respect to load current, driver supply voltage, driver gate current, and total circuit inductance in a simple manner.

The MOSFET parasitic capacitances are required in the model. They are estimated using the effective values [1] as follows in (1)–(3), using datasheet specification values for $v_{ds1\_spec}, C_{rss1\_spec},$ and C_{iss1_spec}. As in [2]–[4], the C_{ds1} capacitor of the synchronous buck HS MOSFET is neglected in the proposed model since it has minimal impact on switching loss, and inclusion greatly complicates the modeling process

$$C_{gd1} = 2C_{rss1\_spec}\sqrt{\frac{V_{ds1\_spec}}{V_{\rm in}}} \tag{1}$$

$$C_{iss1} = C_{iss1\_spec} \tag{2}$$

$$C_{gs1} = C_{iss1} - C_{gd1}. \tag{3}$$

In the following three sections, derivations of the model for the turn-on, turn-off, and the total switching loss are presented.

A. Turn-On Switching Loss Model

Piecewise linear turn-on waveforms of $i_{ds1}, v_{ds1},$ and v_{gs1}, and the power loss in M_1 and P_{M1} are provided in Fig. 7. These waveforms and knowledge of the circuit operation are used extensively in this section in order to derive the turn-on loss $P_{\rm ON}$.

By definition, $P_{\rm ON}$ is derived using the simple integral in (4), representing the average power over one switching period

$$P_{\rm ON} = f_s \int_0^{T_r} v_{ds1} i_{ds}\, dt = \frac{1}{6} V_{\rm in} I_{\rm ON} T_r f. \tag{4}$$

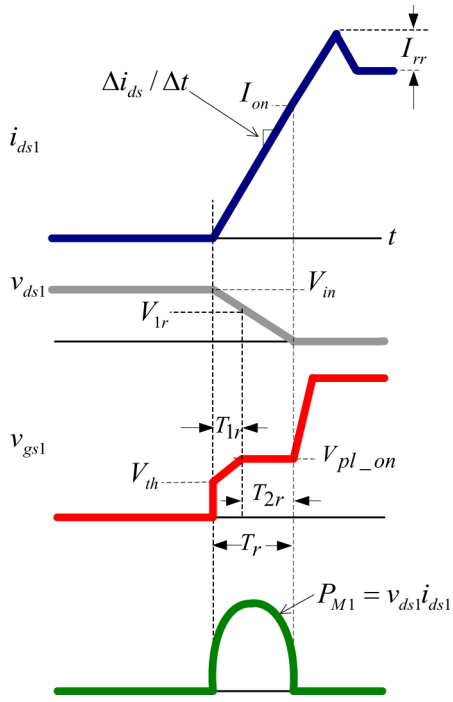


Fig. 7. Synchronous buck HS MOSFET waveforms at turn-on with piecewise linear approximations.

The power loss in (4) is the product of $V_{\rm in}, I_{\rm ON}, f_s,$ and T_r. The turn-on current, $I_{\rm ON}$ is the HS MOSFET drain current when $v_{ds1} = 0$. The two parameters that are key to accurate prediction of $P_{\rm ON}$ are the current at turn-on $I_{\rm ON}$ and T_r. The remainder of this section provides a simple procedure to calculate $I_{\rm ON}$ and T_r, to enable the calculation of $P_{\rm ON}$.

T_r is dictated by the gate driver's ability to charge the MOSFET gate capacitances, which is the time for v_{ds1} to fall to zero. This time is assumed to be independent of the time it takes i_{ds1} to rise to its final value. Under this assumption, T_r consists of two intervals T_{1r} and T_{2r}, which are discussed in the following sections.

1) Rise Time Interval T_{1r}: Charging HS MOSFET C_{gs1} and C_{gd1} Gate Capacitances.

The HS MOSFET equivalent circuit during T_{1r} is given in Fig. 8. The gate resistance R_r represents the total series resistance in the gate drive path, i.e., $R_r = R_{\rm hi} + R_{\rm ext} + R_g$, where $R_{\rm hi}$ is the resistance of the driver switch, $R_{\rm ext}$ is any external resistance, and R_g represents the internal gate resistance of the MOSFET.

During T_{1r}, the C_{gs1} capacitance is charged from $V_{\rm th}$ to $V_{\rm pl\_ON}$, while the gate side of C_{gd1} charges from $V_{\rm th}$ to $V_{\rm pl\_ON}$ and the drain side of the C_{gd1} capacitance discharges from $V_{\rm in}$ to V_{1r}. Therefore, the change in voltage across C_{gd1} during T_{1r} is $[(V_{\rm in} - V_{1r}) + (V_{\rm pl\_ON} - V_{\rm th})]$. Then, T_{1r} is given by (5), assuming an average gate charging current I_{g1r}. $V_{\rm pl\_ON}$ represents the plateau voltage at turn-on and is given by (6), where Δi_{L_f} represents the buck output inductor-ripple current. Since the peak MOSFET current at turn-on is lower than at turn-off, the plateau voltage at turn-on differs slightly than at

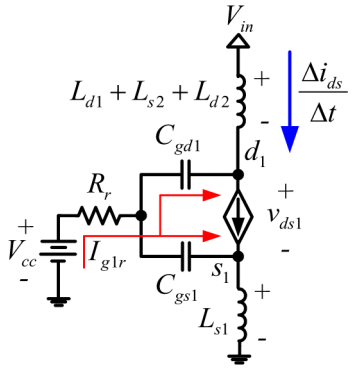


Fig. 8. Synchronous buck HS MOSFET equivalent circuit during T_{1r}.

turn-off. In (5), $\Delta V_{gsr} = V_{\text{pl\_ON}} - V_{\text{th}}$

$$T_{1r} = \frac{C_{gs1}\Delta V_{gsr} + C_{gd1}[\Delta V_{gsr} + (V_{\text{in}} - V_{1r})]}{I_{g1r}} \quad (5)$$

$$V_{\text{pl\_ON}} = V_{\text{th}} + \frac{I_o - 0.5\,\Delta i_{Lf}}{g_{fs}}. \quad (6)$$

The drain–source voltage during T_{1r} is given by (7), where $L_{\text{loop}} = L_{s1} + L_{d1} + L_{s2} + L_{d2}$

$$v_{ds1} = V_{\text{in}} - L_{\text{loop}}\frac{di_{ds1}}{dt}. \quad (7)$$

The rate of change of drain current in (7) is given by (8) using the piecewise linear approximation of the gate–source voltage waveform during T_{1r}

$$\frac{\Delta i_{ds}}{\Delta t} = \frac{dg_{fs}(v_{gs1} - V_{\text{th}})}{dt} = \frac{g_{fs}\Delta V_{gsr}}{T_{1r}}. \quad (8)$$

Using (8), the intermediate voltage V_{1r} is given by (9)

$$V_{1r} = V_{\text{in}} - L_{\text{loop}}\frac{g_{fs}\Delta V_{gsr}}{T_{1r}}. \quad (9)$$

The driver equivalent circuit during T_{1r} is illustrated in Fig. 9(a) and the gate–source voltage waveform is provided in Fig. 9(b). During this time interval, it is assumed that v_{gs1} is the average value of the plateau $V_{\text{pl\_ON}}$ and threshold voltages V_{th}. In addition, in the proposed model, the slope of the drain current is assumed constant; therefore, the voltage $v_{Ls1} = L_{s1}\Delta i_{ds}/\Delta t$ is constant; so the L_{s1} inductance is replaced by an ideal voltage source in the drive circuit. The average gate current, during T_{1r}, using the linearized v_{gs1} waveform is given by

$$I_{g1r} = \frac{V_{cc} - 0.5(V_{\text{pl\_ON}} + V_{\text{th}}) - L_{s1}(\Delta i_{ds}/\Delta t)}{R_r}. \quad (10)$$

Solving for T_{1r} using (5), (9), and (10) yields (11), where $V_{gs1r} = 0.5(V_{\text{pl\_ON}} + V_{\text{th}})$, (11) as shown at the bottom of this page.

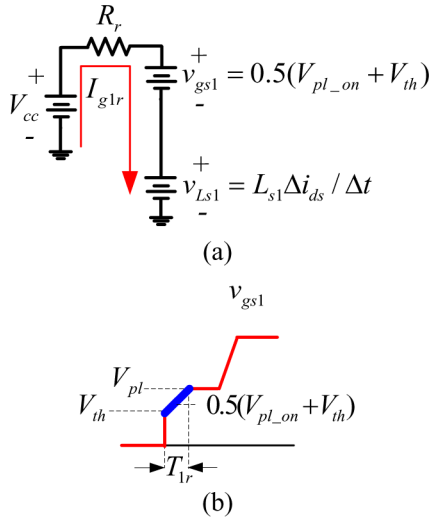


Fig. 9. Driver equivalent circuit during T_{1r}.

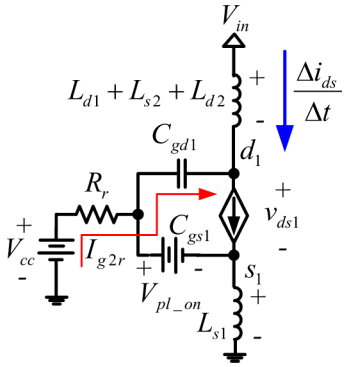


Fig. 10. Synchronous buck HS MOSFET equivalent circuit during T_{2r}.

2) Rise Time Interval T_{2r}: Charging the HS MOSFET C_{gd_1} Gate Capacitance.

The HS MOSFET equivalent circuit during T_{2r} is given in Fig. 10.

During T_{2r}, the gate voltage of the C_{gd1} capacitance remains constant at $V_{\text{pl\_ON}}$, while the drain node of C_{gd1} is discharged by current I_{g2r}, allowing T_{2r} to be given by

$$T_{2r} = \frac{C_{gd1}V_{1r}}{I_{g2r}}. \quad (12)$$

The driver equivalent circuit during T_{2r} is illustrated in Fig. 11(a) and the gate–source voltage waveform is provided in Fig. 11(b). Due to the assumed constant $\Delta i_{ds}/\Delta t$, the L_{s1} inductance is replaced by an ideal voltage source. Under these assumptions, the gate current is given by

$$I_{g2r} = \frac{V_{cc} - V_{\text{pl\_ON}} - L_{s1}(\Delta i_{ds}/\Delta t)}{R_r}. \quad (13)$$

$$T_{1r} = \frac{\Delta V_{gsr}(L_{s1}g_{fs} + R_r C_{iss1}) + \sqrt{[\Delta V_{gsr}(L_{s1}g_{fs} + R_r C_{iss1})]^2 + 4\Delta V_{gsr}(V_{cc} - V_{gs1r})R_r C_{gd1} L_{\text{loop}} g_{fs}}}{2V_{gs1r}}. \quad (11)$$

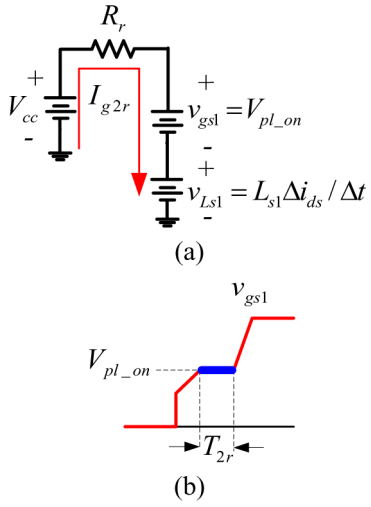


Fig. 11. Driver equivalent circuit during T_{2r}.

Solving for T_{2r} using (9), (12), and (13) yields

$$T_{2r} = \frac{R_r C_{gd1}\left(V_{\text{in}} - L_{\text{loop}} g_{fs}(\Delta V_{gsr}/T_{1r})\right)}{V_{cc} - V_{\text{pl\_ON}} - L_{s1} g_{fs}(\Delta V_{gsr}/T_{1r})}. \tag{14}$$

The total T_r is the sum of T_{1r} and T_{2r}, as given by

$$T_r = T_{1r} + T_{2r}. \tag{15}$$

The final step to determine the turn-on loss is to estimate the current I_{ON} at the end of T_r. Depending on the load current and parasitic inductances, calculating I_{ON} can require estimation of the reverse recovery current I_{rr}. An expression of I_{rr} is provided in (16), where $\Delta i_{ds}/\Delta t$ represents the average rate of increase of the drain current, Q_{rr_spec} represents the datasheet reverse recovery specification at current I_{rr_spec}, and I_o represents the buck converter average load current. The derivation of I_{rr} is provided in the Appendix

$$I_{rr} = \sqrt{\frac{\Delta i_{ds}}{\Delta t}\frac{Q_{rr\_\text{spec}}}{I_{rr\_\text{spec}}}}\, I_o. \tag{16}$$

Since the rise time is dictated by the time for the HS MOSFET voltage v_{ds1} to fall to zero, the current at the end of T_r can be at any value equal to, or less than, the inductor current plus the reverse recovery current (i.e., I_{ON} is not necessarily equal to the inductor current, as in the conventional model [1], or the inductor current plus the reverse recovery current). There are three cases for I_{ON}, as illustrated in Fig. 12.

The first and the most common case is illustrated in Fig. 12(a) where I_{ON} is less than the peak of the turn-on current waveform at the end of T_r. This case occurs under heavy load conditions and/or with typical or large values of parasitic inductances which limit $\Delta i_{ds}/\Delta t$. In this case, the turn-on current is determined by the slope of the current at turn-on multiplied by T_r, as given by the first condition in

$$I_{\text{ON}} = \begin{cases} \frac{\Delta i_{ds}}{\Delta t} T_r, & \text{if } \frac{\Delta i_{ds}}{\Delta t} T_r < I_o - 0.5\Delta i_{Lf} + I_{rr} \\ I_o - 0.5\Delta i_{Lf} + I_{rr}, & \text{otherwise.} \end{cases} \tag{17}$$

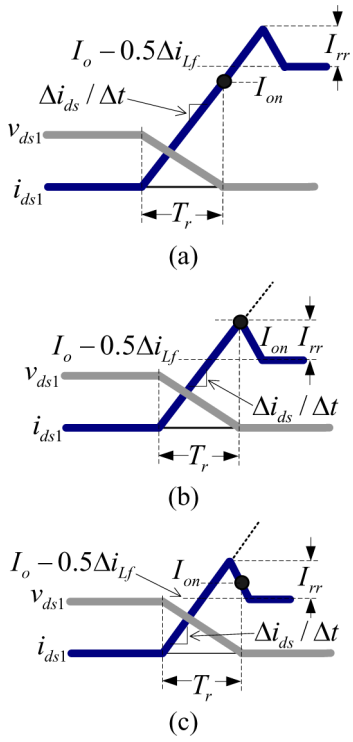


Fig. 12. Three possible cases of turn-on current when $V_{ds1} = 0$. (a) I_{ON} less than I_{ds1} peak value. (b) I_{ON} is equal to the I_{ds1} peak value. (c) I_{ON} occurs after the I_{ds1} peak value.

The first condition holds as long as the calculated value is less than the inductor current ($I_o - 0.5\Delta i L_f$) plus I_{rr}, which leads to the second and third conditions in Fig. 12(b) and (c).

Under light load and/or conditions where the parasitic inductances are small, using the current slope times T_r would yield a turn-on current greater than the peak current and somewhere on the dotted line extensions in Fig. 12(b) and (c). In this case, the current is capped at maximum value of the inductor current plus reverse recovery current, as given by the second condition in (17). The third case, illustrated in Fig. 12(c), occurs under very light-load conditions, and/or when the parasitic inductances are very small. To simplify the model, this case is neglected and if it occurs, the second case in Fig. 12(b) is used as given by the second condition in (17).

The total turn-on switching loss can be calculated using (4), (15), and (17).

B. Turn-Off Switching Loss Model

Piecewise linear turn-off waveforms of i_{ds1}, v_{ds1}, and v_{gs1}, and the power loss in M_1 and P_{M1} are provided in Fig. 13. These waveforms and knowledge of the circuit operation are used extensively in this section in order to derive the turn-off loss P_{OFF}. The turn-off transition consists of two intervals T_{1f} and T_{2f}.

During T_{1f}, the Miller capacitor C_{gd1} is discharged while v_{gs1} remains at $V_{\text{pl\_OFF}}$, and i_{ds1} is assumed to remain constant. In a real circuit, it is noted that i_{ds1} begins to fall during T_{1f}; however, the current slope is limited due to the discharging of

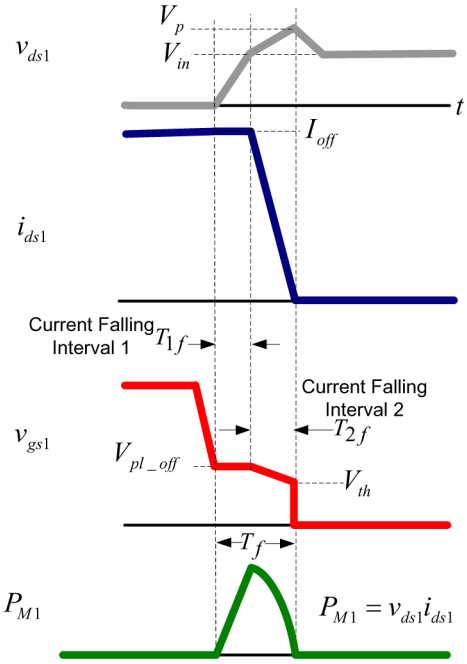


Fig. 13. Synchronous buck HS MOSFET waveforms at turn-off with piecewise linear approximations.

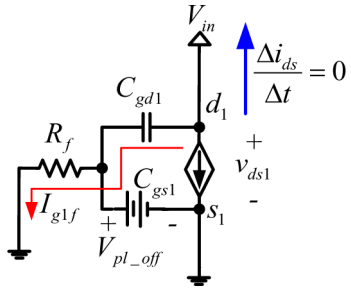


Fig. 14. Synchronous buck HS MOSFET equivalent circuit during T_{1f}.

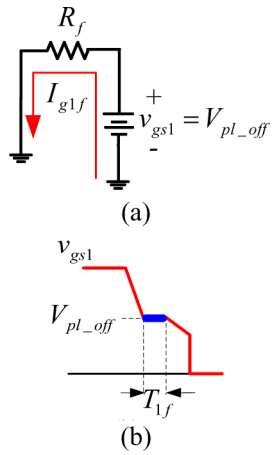


Fig. 15. Driver equivalent circuit during T_{1f}.

the C_{gd2} and C_{ds2} capacitors of the SR. During this interval, v_{ds1} increases from zero to $V_{\rm in}$. Therefore, from the geometry, the turn-off power loss $P_{1\rm OFF}$, during T_{1f}, is given by

$$P_{1\rm OFF} = \frac{1}{2} V_{\rm in} I_{\rm OFF} T_{1f} f_s. \tag{18}$$

During T_{2f}, C_{gs1} is discharged from $V_{\rm pl\_OFF}$ to $V_{\rm th}$, while the gate node of C_{gd1} is also discharged from $V_{\rm pl\_OFF}$ to $V_{\rm th}$, and the drain node of C_{gd1} is charged from $V_{\rm in}$ to the peak voltage at turn-off V_p. During this interval, i_{ds1} falls from $I_{\rm OFF}$ to zero, while v_{ds1} rises from $V_{\rm in}$ to V_p. Using a simple integral following the procedure presented in Section III, the turn-off loss during T_{2f} is approximated as $P_{2\rm OFF}$, given by

$$P_{2\rm OFF} = \left(\frac{1}{6}(V_p - V_{\rm in}+) I_{\rm OFF} + \frac{1}{2} V_{\rm in} I_{\rm OFF} \right) T_{2f} f_s. \tag{19}$$

The total turn-off loss $P_{\rm OFF}$ is the sum of $P_{1\rm OFF}$ and $P_{2\rm OFF}$

$$P_{\rm OFF} = P_{1\rm OFF} + P_{2\rm OFF}. \tag{20}$$

The key parameters to accurate prediction of the turn-off loss are the HS MOSFET current at turn-off $I_{\rm OFF}$, the intervals T_{1f} and T_{2f}, and the peak overshoot voltage of v_{ds1}, V_p. The turn-off current is the load current I_o plus half of the filter inductor peak-to-peak ripple current Δi_{L_f}, as given by

$$I_{\rm OFF} = I_o + \frac{1}{2} \Delta i_{Lf}. \tag{21}$$

The plateau voltage at turn-off $V_{\rm pl\_OFF}$ is given by (23). It differs slightly from $V_{\rm pl\_ON}$ at turn-on due to the larger switch current during the transition

$$V_{\rm pl\_OFF} = V_{\rm th} + \frac{I_o + 0.5\,\Delta i_{Lf}}{g_{fs}}. \tag{22}$$

The turn-off loss estimated using (20) is a function of T_f. During T_f, the current falls from $I_{\rm OFF}$ to zero and v_{ds1} rises from zero to V_p. It is a function of the driver's capability to discharge C_{gd1} and C_{iss1}, but in addition, it is a function of circuit parasitic inductances that limit the current falling slope, and therefore, the falling time.

1) Fall Time Interval T_{1f} (Discharging the HS MOSFET C_{gd_1} Gate Capacitance): The HS MOSFET equivalent circuit during T_{1f} is given in Fig. 14. Since i_{ds1} remains constant at $I_{\rm OFF}$ (also illustrated in Fig. 13 during interval T_{1f}), $\Delta i_{ds}/\Delta t = 0$, so the parasitic inductors can be neglected. The variable T_{1f} is the time required to discharge the C_{gd1} capacitance by gate current I_{g1f}, as given by

$$T_{1f} = \frac{C_{gd1} V_{\rm in}}{I_{g1f}}. \tag{23}$$

The driver equivalent circuit during T_{1f} is illustrated in Fig. 15(a) and the gate–source voltage waveform is provided in Fig. 15(b). During this time interval, it is assumed that v_{gs1} remains constant at the plateau $V_{\rm pl\_OFF}$. With this assumption, the gate current is easily derived as given by (24), where

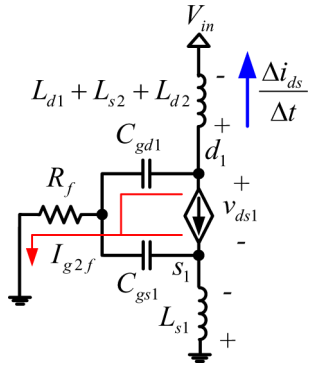


Fig. 16. Synchronous buck HS MOSFET equivalent circuit during T_{2f}.

$R_f = R_{l_o} + R_{\text{ext}} + R_g$, and $V_{\text{pl\_OFF}}$ is given by (22)

$$I_{g1f} = \frac{V_{\text{pl\_OFF}}}{R_f}. \tag{24}$$

Using (23) and (24), T_{1f} is given by

$$T_{1f} = \frac{C_{gd1} V_{\text{in}} R_f}{V_{\text{pl\_OFF}}}. \tag{25}$$

2) Fall Time Interval T_{2f} (Current Falling and Discharging the HS MOSFET C_{gs1} and C_{gd1} Gate Capacitances): The HS MOSFET equivalent circuit during T_{2f} is given in Fig. 16. During T_{2f}, the C_{gs1} capacitance is discharged from $V_{\text{pl\_OFF}}$ voltage to V_{th}, while the voltage at the drain side of the C_{gd1} capacitance charges from V_{in} to V_p, and the voltage at the gate side of C_{gd1} discharges from $V_{\text{pl\_OFF}}$ to V_{th}. Therefore, the change in voltage across C_{gd1} during T_{2f} is $[(V_p - V_{\text{in}}) + (V_{\text{pl\_OFF}} - V_{\text{th}})]$. Then, T_{2f} is given by (26), where $\Delta V gsf = V_{\text{pl\_OFF}} - V_{\text{th}}$

$$T_{2f} = \frac{C_{gs1}\Delta V_{gsf} + C_{gd1}[(V_p - V_{\text{in}}) + \Delta V_{gsf}]}{I_{g2f}}. \tag{26}$$

The drain–source voltage during T_{2f} is given by (27), where $L_{\text{loop}} = L_{s1} + L_{d1} + L_{s2} + L_{d2}$

$$v_{ds} = V_{\text{in}} + L_{\text{loop}} \frac{di_{ds1}}{dt}. \tag{27}$$

Following the approach of the approximations made in (8), the peak overshoot voltage V_p is given by

$$V_p = V_{\text{in}} + L_{\text{loop}} \frac{g_{fs}\,\Delta V_{gsf}}{T_{2f}}. \tag{28}$$

The driver equivalent circuit during T_{2f} is illustrated in Fig. 17(a) and the gate–source voltage waveform is provided in Fig. 17(b). During this time interval, it is assumed that v_{gs1} is the average value of the plateau $V_{\text{pl\_OFF}}$ and threshold voltages V_{th}. As before, the L_{s1} inductance is replaced by an ideal voltage source, where di_{ds}/dt is assumed constant at $g_{fs}\Delta V_{gsf}/T_{2f}$.

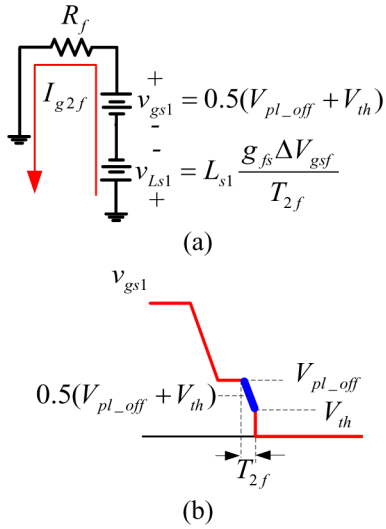


Fig. 17. Driver equivalent circuit during T_{2f}.

With these assumptions, the average gate current during T_{2f}, using the linearized v_{gs1} waveform, is given by

$$I_{g2f} = \frac{(1/2)(V_{\text{pl}} + V_{\text{th}}) - L_{s1}(g_{fs}\,\Delta V_{gsf}/T_{2f})}{R_f}. \tag{29}$$

Solving for T_{2f} using (26), (28), and (29) yields (30), given at the bottom of this page, where $V_{gs2f} = 0.5(V_{\text{pl\_OFF}} + V_{\text{th}})$.

T_f is the sum of T_{1f} and T_{2f}, as given by (31). The total turn-off switching loss can be calculated using (18)–(22), (25), (28), (30), and (31)

$$T_f = T_{1f} + T_{2f}. \tag{31}$$

C. Total Switching Loss Model

The total switching loss, given by (32), is the sum of the turn-on loss P_{ON}, given by (4), and turn-off loss P_{OFF}, given by (20)

$$P_{\text{tot\_sw}} = P_{\text{ON}} + P_{\text{OFF}}. \tag{32}$$

IV. Model Verification

The analytical switching loss model with voltage source drive was compared to SIMetrix Spice simulation and the conventional model in [1]. Simulation results were conducted at 12-V input, 1 MHz switching frequency, and 10-A peak-to-peak buck output inductor ripple (100 nH), $R_{\text{hi}} = 2\ \Omega$, $R_{lo} = 2\ \Omega$, $R_g = 1\ \Omega$, $R_{\text{ext}} = 0\ \Omega$. MOSFET parameters: M_1: Si7860DP, $g_{fs} = 60$ S, $V_{\text{th}} = 2$ V, $C_{iss1\_\text{spec}} = 1800$ pF (at $V_{ds1\_\text{spec}} = 15$ V), $C_{oss1\_\text{spec}} = 600$ pF (at $V_{ds1\_\text{spec}} = 15$ V), $C_{rss1\_\text{spec}} = 200$ pF (at $V_{ds1\_\text{spec}} = 15$ V), and M_2: Si7336ADP SR, $Q_{rr\_\text{spec}} = 30$ nC, $I_{rr\_\text{spec}} = 25$ A.

$$T_{2f} = \frac{\Delta V_{gs2f}(L_{s1}g_{fs} + R_f C_{iss1}) + \sqrt{\Delta V_{gs2f}^2[L_{s1}g_{fs} + R_f C_{iss1}]^2 + 4\,\Delta V_{gs2f} V_{gs2f} R_f C_{gd1} L_{\text{loop}} g_{fs}}}{2V_{gs2f}}. \tag{30}$$

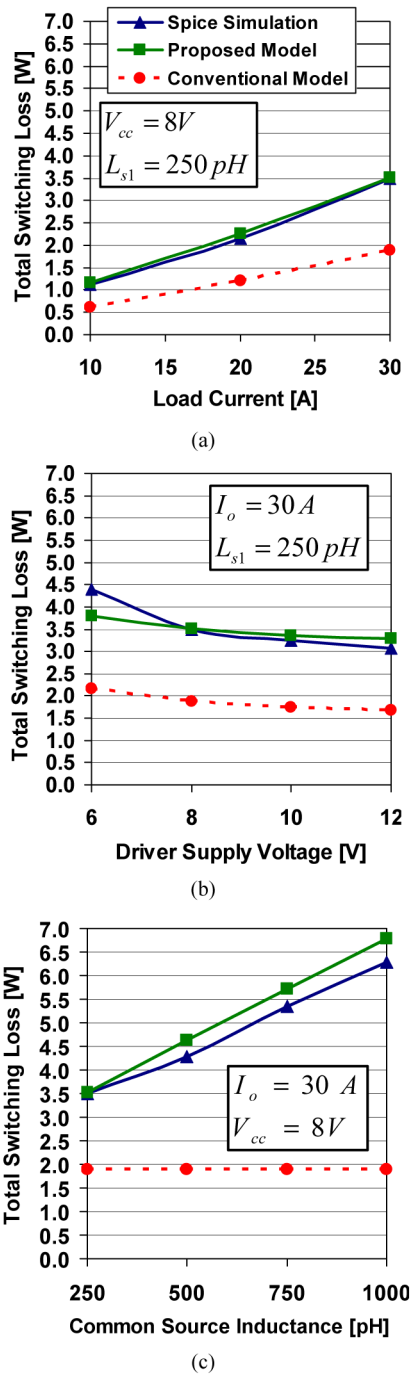


Fig. 18. Total switching loss at 1 MHz, 12-V input as a function of (a) load current ($V_{cc} = 8$ V, $L_{s1} = 250$ pH); (b) driver supply voltage ($I_o = 30$ A, $L_{s1} = 250$ pH); and (c) common source inductance ($V_{cc} = 8$ V, $I_o = 30$ A).

Curves of total switching loss as a function of: 1) load current; 2) driver supply voltage; and 3) common source inductance (assuming matched inductances, i.e., $L_{s1} = L_{d1} = L_{s2} = L_{d2}$) for the proposed model, Spice simulation, and conventional model are given in Fig. 18(a)–(c). The proposed model follows the trends of the Spice simulation results very well. The accuracy of the proposed model total switching loss is within 0.5 W for all conditions. In Fig. 18, it is noted that the conventional model does a very poor job predicting the total switching loss in all three cases, but in particular as total circuit inductance increases. Specifically, at 1000 pH in Fig. 18(c), the conventional model predicts 2.0 W loss, while the Spice results indicate total switching loss of 6.3 W—a difference of 4.3 W. The results also show that the total switching loss can be reduced by increasing V_{cc}. However, for $V_{cc} > 8$ V, the reduction is not significant.

Curves of the turn-on and turn-off switching loss components loss as a function of: 1) load current; 2) driver supply voltage; and 3) common source inductance for the proposed model, Spice simulation, and conventional model are given in Fig. 19(a)–(c) and Fig. 20(a)–(c), respectively. The proposed model follows the trends of the Spice simulation results. In particular, the proposed model correctly predicts that the turn-off loss increases with common source inductance since T_f increases significantly with L_{s1}. In the conventional model, turn-off switching loss remains constant with common source inductance leading to an error in predicted loss of over 4.6 W at 1000 pH in Fig. 20(c). The results also show that turn-on loss decreases with V_{cc}, as expected, since increasing V_{cc} provides increasing driver source current. In contrast, the turn-off loss remains constant with V_{cc}, since the driver sink current is determined by $V_{\mathrm{pl\_OFF}}$.

V. Experimental Results

Experimental results were presented in Section II to aid in demonstrating the switching loss characteristics as load and common source inductance change. These results were presented at low frequency with a large inductance wire introduced in series between the source and common point on the driver in order to measure the HS MOSFET current and demonstrate the trends. However, since probing the MOSFET current is impractical in a real VR with good layout, therefore, the actual switching loss in the prototype cannot be measured; so a direct comparison between the modeled switching loss and actual switching loss cannot be made.

Given the constraints on measuring actual switching loss, another method to gauge the accuracy of the proposed model is to use it in a loss analysis file that estimates the switching loss, other losses and total loss for a synchronous buck VR, and compare it to the total loss in the real circuit. This analysis has been completed, and the total loss in the design file has been compared to the total measured loss of the circuit by subtracting the load power from the input power.

Circuit parameters: 1 MHz switching frequency; 12-V input; 1.3-V output; 330-nH buck inductor; $V_{cc} = 10$ V; IRF6617 HS MOSFET : $g_{fs} = 39$ S, $V_{\mathrm{th}} = 1.85$ V, $C_{rss1\_\mathrm{spec}} = 160$ pF (at $V_{ds1\_\mathrm{spec}} = 15$ V), $C_{oss\_\mathrm{spec1}} = 450$ pF (at $V_{ds1\_\mathrm{spec}} = 15$ V), $C_{iss1\_\mathrm{spec}} = 1300$ pF (at $V_{ds1\_\mathrm{spec}} = 15$ V), and IRF6691 SR MOSFET; $L_{s1} = L_{d1} = L_{s2} = L_{d2} = 500$ pH (model). Driver parameters: UCC27222 driver (experimental); $R_{\mathrm{hi}} = 1.8\ \Omega$, $R_{\mathrm{lo}} = 1.8\ \Omega$, $R_g = 1\Omega$, $R_{\mathrm{ext}} = 0\ \Omega$ (model).

The estimated synchronous buck VR losses and model predicted switching loss as a function of load current is compared to the experimentally measured loss in Fig. 21 for the voltage source driver. Good agreement is achieved between the loss

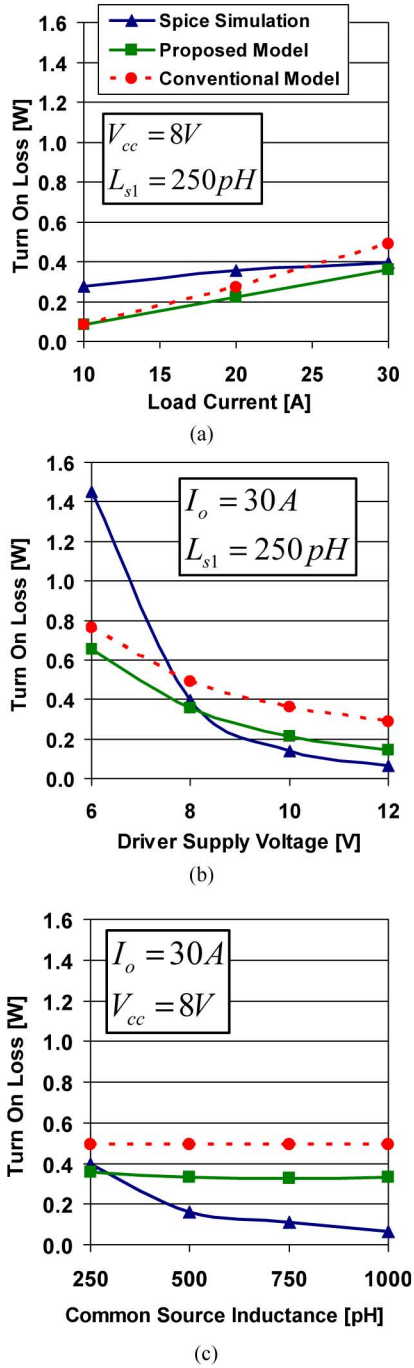


Fig. 19. Turn-on switching loss at 1 MHz, 12-V input as a function of (a) load current ($V_{cc} = 8$ V, $L_{s1} = 250$ pH); (b) driver supply voltage ($I_o = 30$ A, $L_{s1} = 250$ pH); and (c) common source inductance ($V_{cc} = 8$ V, $I_o = 30$ A).

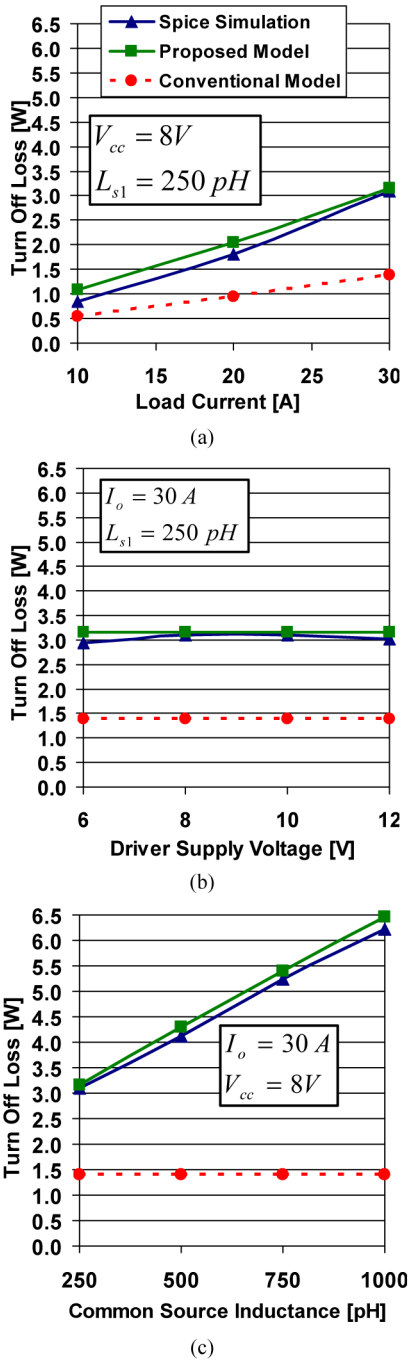


Fig. 20. Turn-off switching loss at 1 MHz, 12-V input as a function of (a) load current ($V_{cc} = 8$ V, $L_{s1} = 250$ pH); (b) driver supply voltage ($I_o = 30$ A, $L_{s1} = 250$ pH); and (c) common source inductance ($V_{cc} = 8$ V, $I_o = 30$ A).

predicted by the model and the actual loss of the VR, with the accuracy within 0.7 W over the entire load range.

A loss breakdown of the estimated losses used to generate the model-predicted loss in Fig. 21 is given in Fig. 22 for 25 A load current. The only losses that can be experimentally measured are the gate and driving power and the input power, which includes the remaining losses (i.e., all except gate and driving).

VI. Current Source Drive Model

A. Current Source Drive Derivation

The proposed model can be extended to the current source drivers presented in [8], [9], and [11]–[13]. These drivers are designed to operate with nearly constant current supplied to the power MOSFET gate. The advantage of this class of drivers is that they eliminate the back voltage v_{Ls1} in the gate circuit that reduces the gate current in conventional voltage source gate drivers.

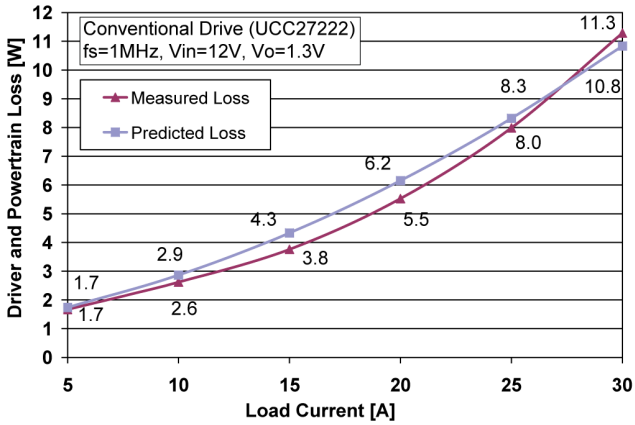


Fig. 21. Comparison of total loss predicted and measured for voltage–source drive (UCC27222, $fs = 1$ MHz, $V_{\rm in} = 12$ V, and $V_o = 1.3$ V).

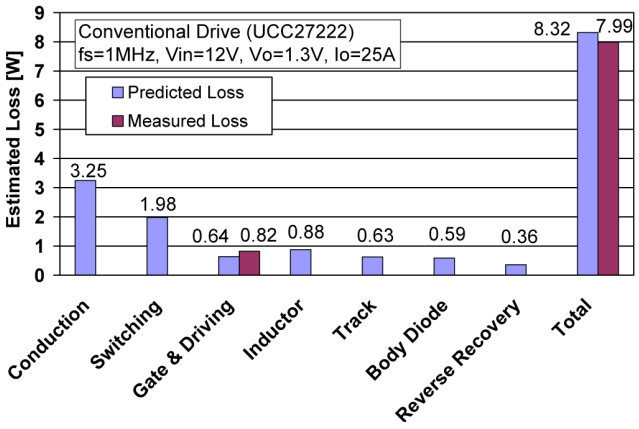


Fig. 22. Loss breakdown of the losses predicted and comparison to the measured gate and total losses for voltage source drive (UCC27222, $fs = 1$ MHz, $V_{\rm in} = 12$ V, and $V_o = 1.3$ V).

With current source drive, determining the rise and fall time intervals is very simple. In this case, the gate current expressions I_{g1r} in (10), I_{g2r} in (13), I_{g1f} in (24) and (29) can all be replaced by a constant gate current with magnitude I_g. At turn-on, T_{1r} in (11) becomes (33) and T_{2r} in (14) becomes (34)

$$T_{1r} = \frac{C_{iss1} + \sqrt{(\Delta V_{gsr} C_{iss1})^2 + 4 I_g \, \Delta V_{gsr} C_{gd1} L_{\rm loop} g_{fs}}}{2 I_g} \tag{33}$$

$$T_{2r} = \frac{C_{gd1} \left(V_{\rm in} - L_{\rm loop} g_{fs} (\Delta V_{gsr} / T_{1r})\right)}{I_g}. \tag{34}$$

At turn-off, T_{1f} in (25) becomes (35) and T_{2r} in (30) becomes (36)

$$T_{1f} = \frac{C_{gd1} V_{\rm in}}{I_g} \tag{35}$$

$$T_{2f} = \frac{\Delta V_{gsf} C_{iss1} + \sqrt{(\Delta V_{gsf} C_{iss1})^2 + 4 I_g \Delta V_{gsf} C_{gd1} L_{\rm loop} g_{fs}}}{2 I_g}. \tag{36}$$

The total turn-on switching loss can be calculated using (4), (15), (17), (33), and (34). The total turn-off switching loss can be calculated using (18)–(22), (28), (31), (35), and (36). The total switching loss, given by (32), is the sum of the turn-on loss $P_{\rm ON}$, given by (4), and turn-off loss $P_{\rm OFF}$, given by (20).

B. Current Source Drive Verification

Curves of total switching loss as a function of: 1) load current; 2) driver supply current; and 3) common source inductance (assuming matched inductances, i.e., $L_{s1} = L_{d1} = L_{s2} = L_{d2}$) for the proposed model, Spice simulation, and the conventional model are given in Fig. 23(a)–(c). The proposed model follows the trends of the Spice simulation results very well. The accuracy of the proposed model total switching loss is within 0.5 W under all conditions. In Fig. 23, it is noted that the conventional model does a poor job predicting the total switching loss in all three cases, but in particular as total circuit inductance increases. The simulation parameters are the same as those provided in Section IV.

C. Current Source Drive Experimental Validation

The estimated synchronous buck VR losses and model-predicted switching loss as a function of load current is compared to the experimentally measured loss in Fig. 24 for the current source driver. Good agreement is achieved between the loss predicted by the model and the actual loss of the VR, with the accuracy within 1 W over the entire load range.

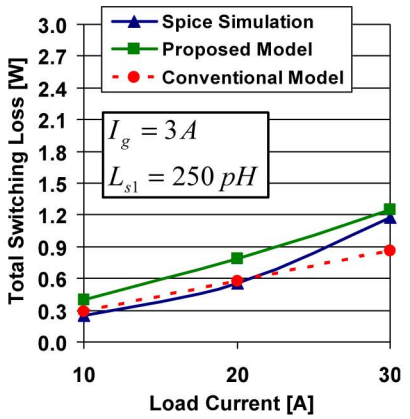
Current source driver parameters: 3 A gate current, 68 nH inductor for the HS MOSFET, 1.3 A gate current, 307 nH inductor for the SR, NDS351AN driver switches with all other parameters the same as those stated in Section V.

A loss breakdown of the estimated losses used to generate the model predicted loss in Fig. 24 is given in Fig. 25 for 25 A load current.

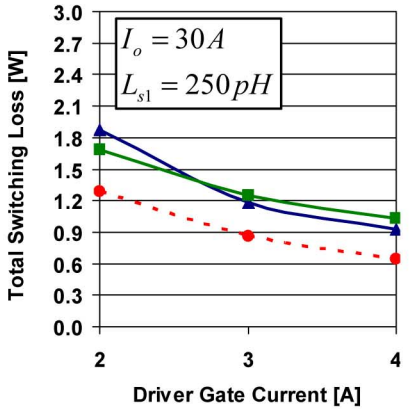
VII. Conclusion

The switching loss characteristics and behavior in a high-frequency synchronous buck VR have been reviewed. The key points to note are: 1) the rise time T_r is dictated by the voltage falling time, which is dictated by the MOSFET parasitic capacitances and current driving capability of the driver; 2) the fall time T_f is dictated by the current falling time, which is dictated by the MOSFET parasitic capacitances and current driving capability of the driver and by the circuit parasitic inductances; and 3) The parasitic inductances act as a current snubber at turn-on to reduce turn-on loss, but prolong T_f to increase turn-off loss.

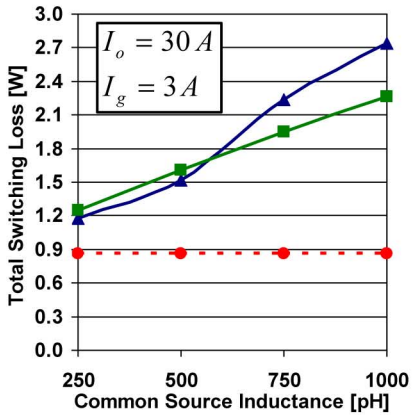
Following the demonstrated switching loss characteristics, a new practical analytical switching loss model has been proposed for voltage source drivers and current source drivers. The model can accurately predict the switching loss in a high-frequency synchronous buck VR using relatively simple closed-form equations. This enables engineers to use a spreadsheet design file to estimate losses in their designs. The proposed model uses piecewise linear approximations of the actual v_{ds1} and i_{ds1} switching



(a)



(b)



(c)

Fig. 23. Total switching loss at 1 MHz, 12-V input as a function of (a) load current ($I_g = 3$ A, $L_{s1} = 250$ pH); (b) driver supply current ($I_o = 30$ A, $L_{s1} = 250$ pH); and (c) common source inductance ($I_g = 3$ A, $I_o = 30$ A).

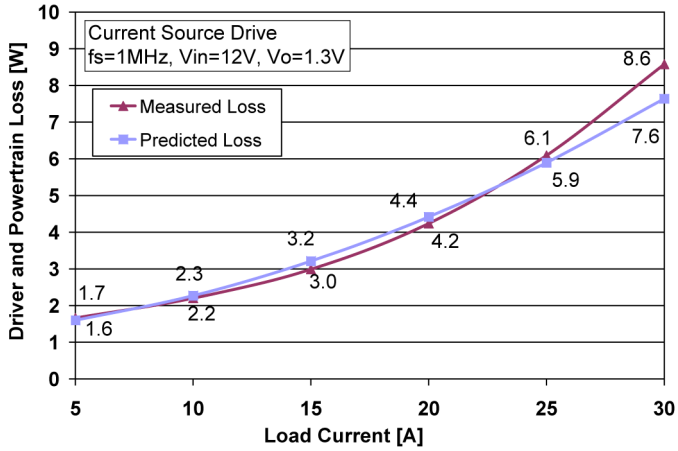


Fig. 24. Comparison of total loss predicted and measured for current source drive ($fs = 1$ MHz, $V_{\text{in}} = 12$ V, and $V_o = 1.3$ V).

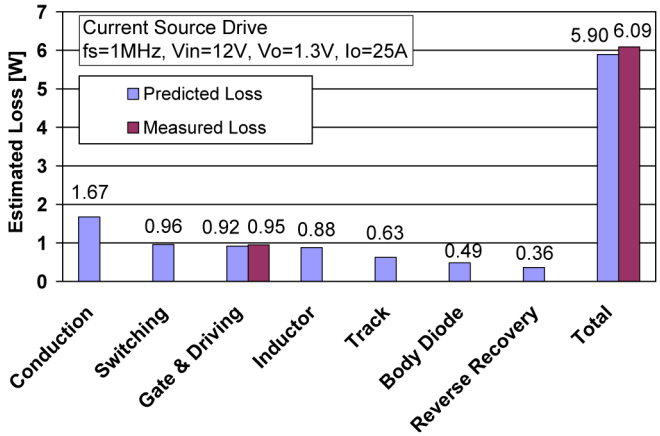


Fig. 25. Loss breakdown of the losses predicted and comparison to the measured gate and total losses for current source drive ($fs = 1$ MHz, $V_{\text{in}} = 12$ V, and $V_o = 1.3$ V).

waveforms. The linearized v_{ds1} and i_{ds1} switching waveforms are then used to provide simple expressions for the turn-on and turn-off loss. Neglected in other models, the reverse recovery current is included in the turn-on switching loss calculation. Circuit parasitic inductances are included in the rise and fall time calculations.

To verify the proposed model, the voltage source drive and current source drive versions were compared to Spice simulation results. It was demonstrated that the proposed model follows the trends in turn-on and turn-off switching loss for variations in load current, driver supply voltage, driver supply current, and total circuit inductance. The accuracy of the proposed models was demonstrated to be within 0.5 W between the calculated and simulated values for the voltage source driver and within 0.5 W for the current source driver. Following the simulation results, the proposed model was used in a loss analysis file to accurately predict the total circuit loss for both the voltage and current source drivers. The total predicted circuit loss was within 0.7 W of the measured loss for the voltage source driver and within 1.0 W of the measured loss for the current source driver operating in a synchronous buck VR at 12 V input, 1.3 V output, and 1 MHz switching frequency.

APPENDIX

The waveform in Fig. 26 is used to estimate I_{rr}. When the HS MOSFET turns on, the SR body diode cannot reverse block; so the SR current goes negative and the HS current spikes by the same magnitude. The total reverse recovery time is T_{rr}. The rising slope magnitude is $\Delta i_{ds}/\Delta t$ and the reverse recovery

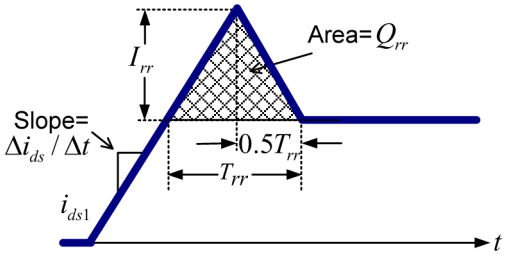


Fig. 26. Synchronous buck HS MOSFET current waveform approximation during reverse recovery at turn-on.

charge is Q_{rr}, which represents the shaded area as given by (37). Using the geometry, the reverse recovery current as a function of T_{rr} is given by (38). Then, eliminating T_{rr} from (37) and (38), (40) is derived, which represents I_{rr} as a function of Q_{rr} and the known slope. In addition, since reverse recovery charge increases with load current, Q_{rr} is approximated using (39), where Q_{rr_spec} and I_{rr_spec} are the datasheet specification values

$$Q_{rr} = \frac{1}{2} I_{rr} T_{rr} \tag{37}$$

$$I_{rr} = \frac{\Delta I_{ds}}{\Delta t} \frac{1}{2} T_{rr} \tag{38}$$

$$Q_{rr} = \frac{Q_{rr\_\text{spec}}}{I_{rr\_\text{spec}}} I_o \tag{39}$$

$$I_{rr} = \sqrt{\frac{\Delta I_{ds}}{\Delta t} Q_{rr}}. \tag{40}$$

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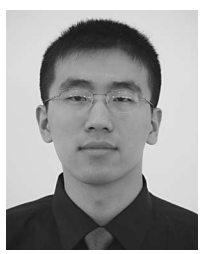

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